

## MULTIPLE PASS OPTIMIZATION FOR AUTOMATIC ELECTRONIC CIRCUIT PLACEMENT

### ABSTRACT

5           A computer implemented process for the automatic creation of integrated  
circuit (IC) geometry including a multiple pass process flow using multiple passes  
of direct timing driven placement after a first pass of non-direct timing driven  
placement. First, a high level description of the circuit design may be synthesized.  
Next, a non-direct timing driven placement process may place the design. Then  
10 the placed design may be routed. Alternatively, routability may be estimated.  
After routing, a modified design may be resynthesized. The resynthesized design  
may then be placed according to a direct timing driven placement process. This  
sequence may be repeated several times.

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